REGISTER CONTROL APPARATUS FOR W-CDMA WLL SEPARATION TYPE TERMINAL

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a wireless communication system, and more particularly to a register control apparatus for a separation type terminal in a wireless communication system.

2. Background of the Related Art

Figure 1 is a block diagram illustrating a CDMA basic type terminal of the background technology. As shown therein, the background W-CDMA basic type terminal includes a microprocessor 11 for controlling operation of a system, a decoding logic unit 12 for decoding a control instruction of the microprocessor 11 and interpreting the decoded instruction signal, and a register 13 for storing data.

The above-described W-CDMA basic type terminal (decoding module 20) includes the decoding logic unit 12 and the register 13 in a module. In addition, there are further provided a modem module, a subscriber interface module, an RF module, etc., which are not shown in Figure 1.

Multiple modules 20 controlled by the microprocessor 11 are connected by a bus and are controlled by a chip select signal, a read signal and a write signal, which are control signals from the microprocessor 11.

The microprocessor 11 reads data stored in the register 13 of each module 20, checks the state of each module 20, writes data used for the next operation into the module register 13, and instructs the next operation of the module.

In the above-described operation, an address bus, a data bus, a chip select signal (CS), a write signal(WR) for writing data into a register, and a read signal(RD) for reading data from the register are used.

In the read operation, the microprocessor 11 generates an RD signal to the module 20 for reading data, and a particular module 20 is selected in accordance with the CS signal. An address which will be read from among the addresses of the register 13 appears at the address bus, and the data read from the register appears at the data bus. At the same time, the data which appears at the data bus is read based on the generated RD signal.

In the write operation, the microprocessor 11 generates a WR signal to the module 20 for writing the data, and the module 20 is selected in accordance with the CS signal. An address which will be written among the addresses of the register 13 appears at the address bus, and the data which will be stored in the register 13 appears at the data bus. The data which appears at the data bus is written into the designated register.

However, in the background method, when the master unit and the slave unit are distanced by a few meters or hundreds of meters like the W-CDMA WLL separation type terminal, the above-described construction results in series problems such as: (1) it is impossible to transmit the address bus, data bus, CS signal, RD signal, and WR signal; and (2) when a new protocol is adapted between the master unit and the slave unit, a new microprocessor is needed in the slave unit for processing the protocol. In addition, in both cases the design of the system must be changed due to the decreased compatibilities with the software.

SUMMARY OF THE INVENTION

An object of the invention is to solve at least the above problems and/or disadvantages and to provide at least the advantages described hereinafter.

Accordingly, it is an object of the present invention to provide a register control apparatus between a master unit and a slave unit for a W-CDMA WLL separation type terminal which is capable of controlling two remote terminals by providing a transmission path between the master unit and the slave unit and sharing data between registers.

To achieve the above object and other objects, there is provided a register control apparatus between a master unit and a slave unit for a W-CDMA WLL separation type terminal which includes a mirror register of a master unit, a register of a slave unit, a framing logic unit for periodically transmitting and extracting data by the master unit and the slave unit through a time slot, and a transmission path for connecting the master unit and the slave unit.

To achieve further objects of the invention, there is provided a method of controlling a slave unit in a separation type terminal in a W-CDMA WLL system wherein data is transmitted between the master unit and the slave unit such that data contained in the master unit is the same as data contained in the slave unit, the slave unit is located remotely from the master unit, and the slave unit is controlled by the master unit based on data stored in the master unit and received from the slave unit.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objects and advantages of the invention may be realized and attained as particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements wherein:

Figure 1 is a block diagram illustrating a background W-CDMA WLL basic terminal; and

Figure 2 is a block diagram illustrating a register control apparatus between a master unit and a slave unit for a W-CDMA WLL according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Figure 2 is a block diagram illustrating an example of a register control apparatus between a master unit 1 and a slave unit 2 for a W-CDMA WLL separation type terminal according to a preferred embodiment of the present invention. As shown therein, the register control apparatus includes a master unit 1, a slave unit 2, and a transmission path 25 connecting the master unit 1 and the slave unit 2.

The master unit 1 includes a microprocessor 21 for controlling the operations of the W-CDMA WLL separation type terminal, a decoding logic unit 22 for decoding control instructions of the microprocessor 21 and interpreting the decoded instruction signal, and a plurality of mirror registers 23 for storing the control instruction of the microprocessor 21 inputted through the decoding logic unit 22 and storing data of the slave unit 2. Also included in master unit 1 is a framing logic unit 24 for periodically transmitting the control instructions of the microprocessor 21 stored in the mirror registers 23 to the slave unit 2 through the transmission path 25 based on a time slot, receiving data of the slave unit 2 inputted through the transmission path 25, extracting the received data and storing the extracted data into the mirror registers 23.

The slave unit 2 includes a plurality of slave registers 26 for storing data and instructing the next instruction, and a framing logic unit 27 for periodically transmitting the data stored in the slave registers 26 to the master unit 1 through the transmission path 25 based on a time slot of the framing logic unit 27, receiving the contents of a mirror register 23 of the master unit 1 and storing the data extracted from the slave registers 26. The operation of slave unit 2 is controlled by the microprocessor 21. Namely, the slave unit 2 operates when the microprocessor 21 writes data into the slave registers 26.

Since the master unit and slave unit are remotely distanced, the transmission path 25 is used for periodically transmitting and receiving the data therebetween. The periodic transmission between the master unit and the slave unit through the allocated time slot is implemented by the framing logic units 24 and 27. The data of the mirror register 23 and the slave register 26 are changed during the above-described process, and the updated data is transmitted therebetween to maintain the same data state in both mirror register 23 and slave register 26.

In the write operation, the microprocessor 21 of the master unit 1 does not directly access the slave register 26 of the slave unit 2, but instead accesses the mirror register 23.

When data is written by the microprocessor 21 into a designated address of the mirror register 23, various buses of the microprocessor 21 write the data into the mirror registers 23 in a manner similar to the background method discussed above.

However, in the present invention, the data written in the mirror register 23 is periodically transmitted to the slave unit 2 through the time slot of the framing logic unit 24. The transmitted data is extracted by the framing logic unit 27 of the slave unit 2 and is written into each slave register 26. The slave unit 2 operates based on the data written in the slave registers 26.

In the read operation, the data of the slave register 26 is periodically transmitted to the master unit 1 through an allocated time slot. In the master unit, the data is extracted from the time slot and is written into each mirror register 23. The microprocessor 21 of the master unit 1 reads the address stored in the mirror register 23 during the read operation in the same manner that the data written in a corresponding slave register 26 is read.

In the present invention, the transmission path 25 between the master unit 1 and the slave unit 2 can be implemented based on an E1(2.048Mbps) link. The states of the mirror registers 23 and the slave registers 26 are periodically transmitted to the corresponding opponents. Namely, in the case that the data of the slave register 26 of the slave unit 2 or the data of the mirror register 23 of the master unit 1 is changed, the changed contents are transmitted between the master unit 1 and the slave unit 2 at a period of 125 □sec. In this way, the data of the mirror register 23 of the master unit 1 and the slave register 26 of the slave unit 2 are updated. The master unit 1 and the slave unit 2 of the W-CDMA WLL terminals periodically transmit and receive the data through the transmission path 25, extract the transmitted and received data, and store the data in a corresponding register. The

master unit 1 then accesses the mirror register 23 instead of the slave register 26 for controlling the slave unit 2.

In addition, the microprocessor 21 of the master unit accesses only the mirror register 23 through the bus, and the slave unit uses only the corresponding slave register 26. Even when two apparatuses are separated from each other, since the microprocessor accesses the mirror register existing at the same address, it is not necessary to change the address map and the protocol. In addition, complete design changes are not needed based on the hardware and software. As the amount of the data is increased, the capacity of the transmission path is increased for compatibility.

As described above, in the present invention, when control of the W-CDMA WLL separation type terminal and two remote apparatuses is needed, the control is implemented through a certain transmission path.

The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures.